Amendments to the Specification.

Please replace the title with the following rewritten title:

- - ~~Electrical Interconnect Structure and~~ A Method of Forming Electrical Interconnects Having Electromigration-Inhibiting ~~Segments~~ Plugs - -

The following new paragraph has been inserted on page 2, between lines 5 and 6:

--This application is a continuation of Application No. 09/735,566 filed December 12, 2000 (Patent No. issued), which is a divisional application of Application No. 09/316,916 filed May 20, 1999 (Patent No. 6,245,996 issued June 12, 2001) which is a continuation of Application No. 08/722,532 filed September 27, 1996, abandoned.--

The paragraph beginning at page 13, line 1 has been amended as follows:

--Referring now to FIG. 1A, a semiconductor structure 10 is shown having a silicon layer 14, and a silicon dioxide layer 16 as shown. A 0.6 micron thick film, or layer 24 of a relatively high electrically conductive material, here an aluminum-copper (A1-Cu) alloy is evaporated over the surface. Other material may be used for film 24, such as Al, Cu, Au, Ag, or their alloys, i.e. the electrically conductive film 24 need not be immune to electromigration. The film 24 alternatively may be a multi-layer structure having one or more additional layers made of conductive materials, such as indicated above, and/or refractory metals or their compounds, such as Ti, W, TiN, TiW, Mo, Ta, or others, which are known to be immune to electromigration at typical operating conditions of silicon integrated circuits. It is noted that the upper surface of film 24 is a planar surface 21.--

The paragraph beginning at page 13, line 15 has been amended as follows:

--Multiple equidistant rows of windows are formed so that they are aligned along the desired paths of conductors. Minimum-width (Wp) windows 25 (i.e. windows 25 formed with the minimum width practical within the photolithography and etch processes available) are opened in conductive film 24 by conventional photolithography and dry etching as shown in

FIG. IA'. Here, Wp=0.25□m. The depth, Dp, of windows is at least as large as the electrical conductor thickness, Dc, here Dp=Dc=0.6□m. Within each conductor path, the windows 25 are spaced at a distance less than, or equal to, a predetermined critical length, Lc, as shown in FIG. 1A'. The length Lc is selected experimentally, as previously described, to prevent electromigration in the relatively high electrically conductive segments 34 to be patterned in conductive film 24, as will be described in detail in connection with FIG. 1D. The electromigration is prevented by creating a backflow in the relatively high electrically conductive segments 34 which counter-balances electromigration flow. In integrated circuits with submicron feature size, Lc>>Wp. Here, Lc is 100 to 300 microns. The number of windows in each of the desired conductor paths is at least (L/Lc)-1, where L is a desired conductor length. The length, Lp, (FIG. 1A') of each one of the windows 25 is selected so as to be at least as large as the desired width, Wc, (FIG. 1D') of relatively high electrically conductive segments 34 to be patterned in conductive film 24, as will be described in detail in connection with FIG. 1D. Here, Wc=0.5□m. The space Ws between windows belonging to neighboring conductors can be as small as allowed by photo-etch (FIG. 1A'). Here, Ws=0.25□m--.

The paragraph beginning at page 14, line 13 has been amended as follows:

--Referring again to FIG. 1A and 1A', after a layer of photoresist, not shown, deposited over the surface of the structure and used to form the windows 25 is stripped off, a refractory metal liner 28 (FIG. 1B) and a metal layer 30 are successively deposited over the structure, filling the windows 25 as shown in FIGS. 1B and 1B' to provide electromigration-inhibiting/electrically conductive plugs 31. Liner 28 is here sputter deposited or chemically vapor deposited, and metal layer 30 is here sputter deposited, chemically vapor deposited, electroplated or electroless plated. The specific resistivity, RHOp, of conductive layer 30 should preferably be ~~less than, or~~ equal to or less than, four times the specific resistivity, RHOo, of relatively high electrically conductive layer 24. While conductive layer 30 does not have to be immune to electromigration, liner 28 does have to be immune to (i.e., act as a barrier against) electromigration, such as a refractory metal. In fact, conductive layer 30 [[may]] need not be different from conductive layer 24. Here, the conductive layer 30 is a 0.4 micron thick layer of tungsten and the liner 28 is here a 0.25 micron thick layer of titanium and titanium nitride. Here, the titanium is .01 microns thick and the titanium nitride is 0.15 microns.--

The paragraph beginning at page 16, line 19 has been amended as follows:

--The relative increase in conductor electrical resistance associated with the electromigration-inhibiting plugs is calculated as (R-Ro)/Ro=RHOpWp/RHOoLc, where R and Ro are, respectively, the resistances of conductor 35 and a same-length conductor without the plugs, and RHOp and RHOo are the specific resistivities of the electromigration-inhibiting conductive material 30 and the relatively high electrically conductive material 24, respectively. Here, RHOp $8x10^{-6}$ Ohm-cm, RHOo=$3xl0^{-6}$ Ohm-cm, Wp=0.25□m [[um]], and Lc=10.0□m[[um]]. Then, (R-Ro)/Ro=$7x10^{-3}$=0.7%. So, the electrical conductors 35 formed by the described method have low electrical resistance, which does not exceed the resistance of solid relatively high electrically conductive conductors by more than 11. With the described method, a planar surface is provided along the conductor film 24 for accurately photolithographically forming equidistant conductors 15 at a distance smaller than a micron.--

The Abstract has been changed as follows (a clean copy of page 32 containing the updated Abstract accompanies this Amendment):

A method is provided for forming ~~integrated circuit~~ an electrical conductors, comprising forming electrically conductive segments incorporating ~~with~~ electromigration-inhibiting~~/electrically conductive~~ plugs. ~~disposed between electrically conductive segments of the electrical conductor. In accordance with such method,~~A row of windows ~~are~~ is formed ~~within~~ in a planar surface. ~~An~~and electromigration-inhibiting~~/electrically conductive~~ material is deposited over the planar surface and ~~through~~ into the windows to ~~fill the windows and thereby~~ provide~~, in such windows, plugs of~~ electromigration-inhibiting~~/electrically conductive material~~ plugs in the windows. The plugs may be formed by depositing an electromigration-inhibiting liner in the windows and then depositing electrically conductive material to fill the windows. Portions of either or both of the plugs and conductive segments are removed such that the plugs and conductive segments have a coplanar surface. The plugs may be formed in windows in an electrically conductive layer defining the conductive segments. Alternatively, windows may be formed in a dielectric layer and the conductive segments formed from electrically conductive material deposited in trenches in the dielectric between neighboring windows, the plugs, conductive segments and dielectric surface being coplanar. Embodiments of the method may be employed in manufacture

of integrated circuit conductors. ~~the electromigration-inhibiting/electrically-conductive material are removed to form the plugs with surfaces co-planar a surface surrounding the plugs. The electrical conductive segments are formed within the same planar surface as the plugs, either before, or after the plug formation. The electrical conductive segments have surfaces co-planar with the plugs, are aligned with and electrically interconnected through the plugs. The plugs are formed at a distance less than, or equal to, the predetermined critical length, L_c, from each other.~~